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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/032,144	ROUSSEL, PATRICE	
	Examiner	Art Unit	
	BENJAMIN P. GEIB	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-23,93-105,107-118 and 121-123* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-23,93-105,107-118 and 121-123* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 19-23, 93-105, 109-120, and 122 are rejected under 35 U.S.C. 102(b) as being anticipated by Abdallah et al., US Patent 6,115,8 12 (herein after Abdallah).

3. Referring to claim 19, Abdallah has taught a method comprising:

storing only a plurality of non-continuous groups of source bits into a plurality of noncontiguous groups of destination storage locations in response to execution of a first instruction that does not specify an order in which the plurality of non-contiguous groups of source bits are to be stored into a plurality of non-contiguous groups of destination storage locations *[Figure 3E, column 6, lines 42-55]*; and

duplicating bits from the plurality of non-contiguous groups of storage locations into groups of destination storage locations adjacent to the non-continuous groups of destination storage locations *[Figure 3E, column 6, lines 42-55, When element 354 is BBDD]*.

4. Referring to claim 20, Abdallah have taught the method of claim 19, as described above, and in which the source bits are stored in a first register *[Figure 3E, column 6, lines 42-55, element 350]*.

5. Referring to claim 21, Abdallah have taught the method of claim 19, as described above, and in which the source bits represent a double-precision floating point value *[column 5, lines 26-40, column 4, lines 25-57]*.

6. Referring to claim 22, Abdallah have taught the method of claim 19, as described above, and in which the source bits are stored in a first memory location *[Figure 3E, column 6, lines 42-55, element 350]*.

7. Referring to claim 23, Abdallah have taught the method of claim 19, as described above, and in which the source bits represent a single-precision floating point value *[column 5, lines 26-40, column 4, lines 25-57]*

8. Referring to claim 93, Abdallah has taught an apparatus comprising:

a first storage area to store a plurality of non-contiguous groups of source bits in response to execution of a first instruction *[Figure 3E, column 6, lines 42-55, elements 350 and 354, When element 354 is BBDD]*; and

a second storage area to store only the plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations and to store contiguous duplicates of the plurality of noncontiguous groups of source bits *[Figure 3E, column 6, lines 42-55, elements 350 and 354, When element 354 is BBDD.]*.

9. Referring to claim 94, Abdallah have taught the apparatus of claim 93, as described above, and wherein the plurality of non-contiguous groups of source bits are to represent a plurality of 32-bit double-precision floating point value *[column 5, lines 26-40, column 4, lines 25-57]*.

10. Referring to claim 95, Abdallah have taught the apparatus of claim 94, as described above, and wherein the first storage area comprises a 128-bit memory location *[column 5, lines 26-40, column 4, lines 25-57, Figure 3E, element 350, Four times thirty-two equals 128.]*.

11. Referring to claim 96, Abdallah have taught the apparatus of claim 94, as described above, and wherein the first storage and second storage areas each comprise a 128-bit register *[column 5, lines 26-40, column 4, lines 25-57, Figure 3E, elements 350 and 354]*.

12. Referring to claim 97, Abdallah have taught the apparatus of claim 93, as described above, and wherein the plurality of non-contiguous groups of source bits comprise four single precision floating point values *[column 5, lines 26-40, column 4, lines 25-57, Figure 3E]*.

13. Referring to claim 98, Abdallah have taught the apparatus of claim 93, as described above, and wherein the second storage area is to store only two of the plurality of noncontiguous groups of source bits and their duplicates *[Figure 3E, column 6, lines 42-55, elements 3 50 and 3 54, When element 3 54 is BBDD only two are stored.]*.

14. Referring to claim 99, Abdallah have taught the apparatus of claim 93, as described above, and wherein the first and second storage areas are to store data corresponding to multimedia instructions *[column 1, lines 5-55]*.

15. Referring to claim 100, Abdallah have taught the apparatus of claim 99, as described above, and further comprising an execution unit to execute the multi-media instructions [Figure 1, element 1 12].

16. Referring to claim 101, Abdallah has taught a system comprising:

a memory to store a plurality of instructions *[Figure 1, element 120]*;

a processor to fetch a first instruction from the memory, wherein the first instruction, if executed by the processor, is to cause the processor to store only a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations and to store contiguous duplicates of the plurality of non-contiguous groups of source bits into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations *[Figure 3E, column 6, lines 42-55, When element 354 is BBDD]*.

17. Referring to claim 102, Abdallah have taught the system of claim 101, as described above, and wherein the plurality of non-contiguous groups of source bits include a least significant 32 source bits *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 350, D]*.

18. Referring to claim 103, Abdallah have taught the system of claim 10 1, as described above, and wherein the plurality of non-contiguous groups of source bits include a most significant 32 source bits *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 350, A]*.

19. Referring to claim 104, Abdallah have taught the system of claim 102, as described above, and wherein the plurality of non-contiguous groups of source bits include a second most significant group of 32 source bits *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 350, A]*.

20. Referring to claim 105, Abdallah have taught the system of claim 103, as described above, and wherein the plurality of non-contiguous groups of source bits include a second least significant group of 32 source bits *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 350, D]*.

21. Referring to claim 109, Abdallah have taught the system of claim 101, as described above, and wherein the processor is to fetch a second instruction from the memory *[Figure 1, element 110]*, the

second instruction to store a first number of non-contiguous duplicates *[Figure 3E, column 6, lines 42-55, When element 354 is DDDD, there are three non-contiguous duplicates i.e. the first and third, the second and fourth and the first and fourth locations.]* of a second number of contiguous groups of source bits *[Figure 3E, column 6, lines 42-55, When element 354 is DDDD, element 350 only has one contiguous group of source bits.]* into a destination storage location *[Figure 3E, column 6, lines 42-55, element 354]*, the first number being larger than the second number *[Three is larger than one.]*.

22. Referring to claim 110, Abdallah has taught a machine-readable medium having stored thereon an instruction, which if executed by a machine, causes the machine to perform a method comprising:

storing bits (31-0) of a source value into bit storage locations (63-32) and (31-0) of a destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is BBDD]*,

storing bits (95-64) of the source value into bit storage locations (127-96) and (95-64) of the destination register, wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is BBDD]*.

23. Referring to claim 111, Abdallah has taught the machine-readable medium of claim 110, as described above, and wherein the source value is stored in a memory location *[Figure 3E, column 6, lines 42-55, element 350]*.

24. Referring to claim 112, Abdallah has taught the machine-readable medium of claim 110, as described above, and wherein the source value is stored in a register *[Figure 3E, column 6, lines 42-55, element 350]*.

25. Referring to claim 113, Abdallah has taught a machine-readable medium having stored thereon an instruction, which if executed by a machine causes the machine to perform a method comprising:

storing bits (63-32) of a source value into bit storage locations (31-0) and (63-32) of a destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is AACC]*,

storing bits (127-96) of the source value into bit storage locations (127-96) and (95-64) of the destination register, wherein the instruction does not include a code to designate the order in which the

source bits are to be stored in the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is AACC]*.

26. Referring to claim 114, Abdallah has taught the machine-readable medium of claim 113, as described above, and wherein the source value is stored in a memory location *[Figure 3E, column 6, lines 42-55, element 350]*.

27. Referring to claim 115, Abdallah has taught the machine-readable medium of claim 113, as described above, and wherein the source value is stored in a register *[Figure 3E, column 6, lines 42-55, element 350]*.

28. Referring to claim 116, Abdallah has taught a machine-readable medium having stored thereon an instruction, which if executed by a machine causes the machine to perform a method comprising:

storing only bits (63-32) of a source value into bit storage locations (127-96) and (63-32) of a destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is CDCD]*,

storing only bits (31-0) of the source value into bit storage locations (31-0) and (95-64) of the destination register, wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is CDCD]*.

29. Referring to claim 117, Abdallah has taught the machine-readable medium of claim 116, as described above, and wherein the source value is stored in a memory location *[Figure 3E, column 6, lines 42-55, element 350]*.

30. Referring to claim 118, Abdallah has taught the machine-readable medium of claim 116, as described above, and wherein the source value is stored in a register *[Figure 3E, column 6, lines 42-55, element 350]*.

31. Referring to claim 119, Abdallah has taught a machine-readable medium having stored thereon an instruction, which if executed by a machine, causes the machine to perform a method comprising:

storing bits [31-0] of a source value into bit storage locations [31-0] of a destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is BBDD]*;

duplicating bits from the bits storage locations [31-0] to bit storage locations [63-32] of the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is BBDD]*;

Storing bits [95-64] of the source value into bit storage locations [95-64] of the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is BBDD]*; and

Duplicating bits from the bit storage locations [95-64] to bit storage locations [127-96] of the destination register, wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is BBDD]*.

32. Referring to claim 120, Abdallah has taught a machine-readable medium having stored thereon an instruction, which if executed by a machine causes the machine to perform a method comprising:

storing bits [63-32] of a source value into bit storage locations [63-32] of a destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is AACC]*;

duplicating bits from the bit storage locations [63-32] to bit storage locations [31-0] of the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is AACC]*;

storing bits [127-96] of the source value into bit storage locations [127-96] of the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is AACC]*; and

duplicating bits from the bit storage locations [127-96] to bit storage locations [95-64] of the destination register, wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register *[Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is AACC]*.

33. Referring to claim 122, Abdallah has taught the method of claim 19, wherein the order in which the non-contiguous groups of source bits are to be stored into the non-contiguous groups of destination storage locations is specific in accordance with the first instruction *[The order is specified in accordance with the SHUFPS instruction; column 6, lines 42-55]*.

Claim Rejections - 35 USC § 103

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. Claims 107, 108, 121, and 123 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abdallah.

36. Referring to claims 107 and 108, Abdallah has taught the systems of claims 104 and 105, as described above. Abdallah has not taught wherein the first instruction is a MOVSHDUP or a MOVSLDUP instruction. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The storing would be performed the same regardless of the name of the instruction. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381,1385,217 USPQ 401,404 (Fed. Cir. 1983)l In re Lowry, 32 F.3d 1579,32 USPQ2d 1031 (Fed. Cir. 1994). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the instructions be labeled anything, including, MOVSHDUP and MOVSLDUP, because merely labeling the instructions differently from that in the prior art would have been obvious. See Gulack cited above.

37. Referring to claim 121, Abdallah has taught the method of claim 19. Because Abdallah has taught that the order in which the non-contiguous groups of source bits are to be stored is flexible, Abdallah not taught that the order in which the non-contiguous groups of source bits are to be stored into the non-contiguous groups of destination storage location is fixed. However, at the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the invention of Abdallah so that the order in which the non-contiguous groups of source bits are to be stored is fixed. The motivation for fixing the order of the groups of source bits to be stored would have been that complexity of the system would have been reduced, thereby increasing processing efficiency.

38. Referring to claim 123, Abdallah has taught the method of claim 19. Because Abdallah has taught that the order in which the non-contiguous groups of source bits are to be stored is flexible, Abdallah not taught that the first instruction is associated with one unique order of in which the non-contiguous groups of source bits are to be stored into the non-contiguous groups of destination storage locations. However, at the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the invention of Abdallah so that the first instruction is associated with one unique order in which the non-contiguous groups of source bits are to be stored into the non-contiguous groups of destination storage locations. The motivation for associating the first instruction with one unique order would have been that complexity of the system would have been reduced, thereby increasing processing efficiency.

Response to Arguments

39. Applicant's arguments filed 09/28/2009 have been fully considered but they are not persuasive.

40. Applicant argues the novelty/rejection of claims 19-23, 93-105, and 109-120, in substance that:

A) “Abdallah merely moves source data into a destination register and does not then duplicate the data moved into the contiguous locations” (Remarks; page 11)

B) “There is also no mention of ‘duplicating bits from the plurality of non-contiguous groups of destination storage locations into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations.’” (Remarks; page 11)

C) “Abdallah fails to disclose 'storing only a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations'" (Remarks, page 11)

D) “Abdallah fails to disclose ‘a first instruction that does not specify an order in which the plurality of non-contiguous groups of source bits are to be stored into the plurality of non-contiguous groups of destination storage locations.'" (Remarks; page 11, continuing on page 12)

41. These arguments are not found persuasive for the following reasons:

Regarding point A), as shown in FIG. 3E and described at column 6, lines 43-55, Abdallah has taught that the data elements of the source operand "may occupy any location of a result data item." Because the data elements may occupy any location, including multiple locations (See examples given at column 6, lines 53-55), the source data elements are duplicated.

Regarding point B), as described above regarding point A), the data elements of the source operand may occupy any location of the result. See FIG. 3E and column 6, lines 43-55. Because the data elements may occupy any location of the result, one result of the SHUFPS instruction is the "duplicating bits from the plurality of non-contiguous groups of destination storage locations into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations" as recited in the claims. This is the case when the source operand is ABCD and the result of the SHUFPS instruction is BBDD (i.e. the 'B' and 'D' elements are duplicated into result locations adjacent to the 'B' and 'D' result elements).

Regarding point C), while, as noted by the Applicant, Abdallah discloses an example result data item of "ABDC," wherein data elements "A" and "B" are contiguous to each other, this is only one possible example of the result data item. In an instance of the SHUFPS instruction that results in "BBDD", only a plurality of non-contiguous groups of source bits are stored into a plurality of non-contiguous groups of destination storage locations as claimed. Therefore, because Abdallah has taught an embodiment that does "store only a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations," Abdallah has taught the limitations as claimed.

Regarding point D), Abdallah is silent on the exact mechanism for specifying the order in which the data elements are stored in the result. Because Abdallah is silent on the order designation does not require that the instruction must include a code to designate the order. For example, the order could be specified by a value stored in a register. Because the argued claim limitation is a negative limitation and nothing in Abdallah contradicts the claims language, Abdallah has taught the invention as claimed.

Conclusion

42. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN P. GEIB whose telephone number is (571)272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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